CDPH-1970-005 illustrates the complexity to be mastered with the avionic system Picture: © Eric Raz/ Eurocopter

Making a MARTE

THE INTRODUCTION OF META ARCHITECTURE CAN REDUCE MAINTENANCE AND DEVELOPMENT COSTS, OBSOLESCENCE MANAGEMENT, AND THE COMPLEX SYSTEMS FOR THE TEST BENCH USER FOR A FULL HELICOPTER RANGE

BY GEORGE AFONSO AND NICOLAS BELANGER

During an aircraft's development phase, the test process is considered a key challenge for safety-critical avionic systems. These systems often operate under complex dynamic conditions and ultimately provide safety, fault tolerance, and deterministic timing.

For a large range of helicopters, the processing of the different system units is verified using several software and hardware environments. By its nature, the test methodology heavily influences the time-to-market and the cost of the final product. Nicolas Belanger, strategy & innovation coordinator for Engineering Service Technologies at Eurocopter, highlights the situation in the avionics landscape: "For years, it has been widely accepted in the avionic test systems community that test benches should be dedicated to a specific helicopter configuration.

"It is certainly time to reassess this situation. We all know the global ratios, the cost of one flight test hour being equivalent to 20 hours on a test bench and 40 hours spent on simulation. This fact provides a strong motivation to increase virtualization on one side and test systems' reconfigurable architectures on the other. If we have in-house dedicated experts, capable of achieving the target of the virtual helicopter challenge, but on the opposite side we do not have the necessary internal expert competency in the derived scientific field of reconfigurable processor architectures, we are dependent on competent partners such as EADS Innovation Works and INRIA to improve and implement them."

Focusing on this issue, a generic test environment that can adapt easily to the helicopter fleet specifics and the unit-under-test (UUT) was proposed. Within this environment, a hybrid CPU/FPGA (field programmable gate array) 'meta architecture' was imagined to design innovative avionic test systems that meet performance and flexibility goals.

Furthermore, an efficient test methodology that favors the reuse of hardware and software models, the adaptability of the system according to the scenario, and the interoperability of heterogeneous units was defined. The whole project shows the strong impact of the test environment to reduce the complexity of the means employed for the test phase. Eurocopter intends to evaluate the operational benefits of this environment, in order for it to be taken into account when designing its next-generation test benches.

Reconfigurable computing

Stephan C. Stilkerich, expert for reconfigurable computing and computational intelligence at EADS Innovation Works, explains, "Reconfigurable computing has a long-standing history in the academic community, but up to now this field suffers from being exploited with respect to industrial applications. Although the reconfigurable computing technology offers interesting and promising architectural and system features, the lack of established and industrial relevant development environments, as well as runtime environments, halted this technology in industry.

"EADS Innovation Works researches and develops in this field to prepare the technology for use within EADS. The program on Pro-Active Test Systems with Eurocopter is an excellent case study, demonstrating the advantages of this technology in an industrial setting and for EADS Innovation Works and Eurocopter to complement their technical expertise."

It all started by pointing out the major limitations of the existing test systems. In present industrial practice, different test benches are used for the verification of various helicopter types, such as EC175 and EC135, and systems, such as the automatic pilot and navigation. Each test bench relies on a specific hardware architecture and software tools. This is due to the heterogeneity of the helicopter components – UUTs, in terms of computing requirements and handled data structures. In addition to this, dedicated avionic I/O boards (Arinc 429, 1553, etc) are required, depending on the UUTs. This test methodology calls for separate teams with different domain experts to achieve the test of each part. The overall avionic system verification is continued through to the first prototype of the helicopter. Today, this test process is very complex and expensive to perform.

Above: Nicolas Belanger, Eurocopter (left) and George Afonso, EADS Innovation Works (right) . Left: the X3

"Due to the present performance requirements, an increase in the computation rates is needed, which is difficult to achieve with affordable VME CPU board constellations"

This project addresses the above test methodology limitations and calls for an innovative avionic test environment. The main objective is to build up a generic test environment by the means of offering more flexibility regarding the selection of the most suitable test system architecture. An efficient test methodology favors the reuse and the interoperability of hardware and software models while switching between different scenarios. Furthermore, automation in the development process is key to increasing the productivity and reducing the cost.

Eurocopter's contributions in the avionic test environment domain can be summarized as follows: First a hybrid CPU/FPGA architecture for the test system was proposed. In fact, today multicore CPUs come with high computation rates while the FPGA offers flexibility and adaptability to the system. Within this environment, great attention has been devoted to the real-time aspect to satisfy tight computing and communication deadlines. The proposal relies on industrial and certified technologies that can be embedded easily on the final avionic product. Second, an efficient methodology that makes profit from the hybrid architecture to adapt the test system according to the target realization was defined. The reuse and the interoperability advantages are ensured in this methodology with the help of the reconfigurable technology.

Hardware architectures

For the past 20 years, the avionic test systems were based on real-time specific hardware architectures such as the well-spread VME CPU boards. The VMEBus is particularly efficient and enables input/output (I/O) event management, multiprocessing synchronization, and transparent access to the different hardware resources. Like most aeronautic companies, Eurocopter has integrated the VMEBus as a standard backbone for the test benches of embedded flight systems. The proprietary test system ARTIST is based on VME technology and the real-time operating system (OS) VxWorks. These technologies have been used for all helicopter benches to validate the avionic equipment.

Due to the present performance requirements, an increase in the computation rates is needed, which is difficult to achieve with affordable VME CPU board constellations. Furthermore, this solution is considered a costly technology to maintain. To overcome these drawbacks, Eurocopter recently decided to move to an improved test system architecture based on a high performance PC workstation solution. Upcoming architectures are based on multicore computers plugged with I/O boards to communicate with the equipment under test.

Eurocopter selected the PEV1100 VME Bridge solution from the Swiss company IOxOS for its interesting capability to preserve test benches' legacy hardware with a view to a shift to more software-based test systems. The PEV1100 enables a local host to interface with a VME64x bus using a PCI Express (PCIe) external cable, which offers transparent access to I/O boards. To achieve higher communication performances, IOxOS Technology developed a dedicated interface between the PCIe and the VME64x bus. This interface is built with the latest FPGA technology to implement PCIe end-point hardware cores.

The usage of multicore hosts enables an immediate computation capacity increase. An important outcome of this transition is the removal of the legacy CPU boards. However, this solution still does not address the increasing hard real-time criteria anticipated for the execution of tomorrow's concurrent tasks, due to the constraints of the OS environments. Furthermore, the solution doesn't tackle the communication latencies between the CPUs and the I/O boards plugged into any backplane. The Eurocopter proposal profits from the available hardware computing resource (FPGA) in order to build adaptive avionic test systems.

George Afonso, embedded and critical systems engineer/PhD at EADS Innovation Works,

Above: Tiger. Picture courtesy Jérôme Deulin

Left: Eurocopter NH90 simulator.

Below: This test loop will be adapted by the system constraints configuring the test scenario, such as time parameters and environmental parameters

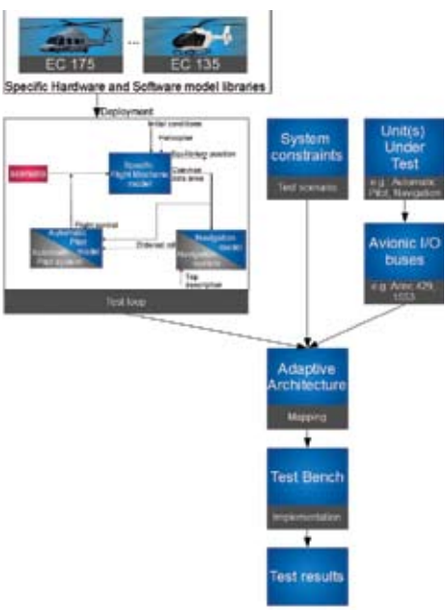
supports FPGA added value for test systems. "Indeed, FPGA technology could offer up to 10 times higher computation rates than CPUs," says Afonso. "It could implement heavy models in a hardware fashion and hide communication latencies with I/O devices."

Adaptive avionic system

To perform a complete simulation, it is necessary to model each part of the helicopter and the environmental parameters, i.e. weather conditions and geographical factors.

The 'test loop' part of the adaptive architecture figure presents a simplified test loop system that simulates the helicopter behavior involving three models: the flight mechanic model, the navigation model, and the automatic pilot model. In the initialization phase, the flight mechanic model takes several parameters such as the initial position relative to the ground and the aircraft configuration file. As a main result, this model gives back an equilibrium position. In addition, it sends the common data area structure containing the position and the speed of the aircraft to the navigation model. This later computes the helicopter destination and sends it to the automatic pilot model via the ordered roll structure. Finally, the flight control is managed by the automatic pilot. Each hardware model, such as the navigation or the automatic pilot, can be replaced by the real hardware-in-the-test-loop.

This test loop will be adapted by the system constraints configuring the test scenario, such as time parameters and environmental parameters, and also by the present UUT. Indeed, the UUT is specific to a helicopter using certain avionic buses. Finally, the UUT will be the main parameter of the architecture configuration, which in Eurocopter's case, is automatic. The main objective of the hybrid architecture is to exploit the new available



hardware computing resource (FPGA) to build up adaptive avionic test systems. The proposed hybrid architecture for the next avionic test systems is composed of multicore CPUs and FPGAs. Our expectation of the above described architecture is to prototype models that can be eligible and relocated in the FPGA.

The objective is to increase the performances of these models and to reduce the communication latencies by the means of embedding the different parts in the same chip. FPGA technology could implement heavy models in a hardware fashion with the management of the parallelism degree to address the real-time constraints of the application. Currently, most of the models are mainly based on software intellectual property (IP).

To obtain fast test system prototyping, heterogeneity of both hardware and software parts had to be dealt with. In current industrial practice, manual coding is still widely adopted in the development of hybrid architectures, which is clearly not suited to manage the complexity intrinsic in these systems.

Rabie Ben Atitallah, researcher at the University of Valenciennes and partner in the project, strongly supports the idea of high-level modeling in the global process. "For designers, manual coding is very tedious, error-prone, and expensive.

"To overcome this challenge, we propose the use of a model-driven engineering (MDE) approach in the specific context of CPU/FPGA hybrid system design," he explains. "The objective is to build a tool that automatically turns a high level specification of the test system into an executable implementation."

Hybrid system modeling

Eurocopter proposes the use of the MARTE standard UML profile to model the hybrid avionic test system. Later, a compilation chain will be defined to turn automatically the high level specification into an executable implementation. With the MARTE specification, an application is a set of tasks connected through ports. Tasks are considered as mathematical functions reading data from their input ports and writing data on their output ports. In addition, MARTE enables the description of the hardware architecture in a structural way. Typical components such as processors, FPGAs, and memory can be specified with their non-functional properties. Furthermore, MARTE provides the 'Allocate' concept as well as 'Distribute', the concept specially crafted for repetitive structures.

This innovative 'meta architecture' will reduce maintenance costs, development costs, obsolescence management, and the complexity to be mastered by the test bench user for a full helicopter range. The next step of the project will deal with event-driven and dynamic reconfiguration of the test environment. The dynamic demonstrator is expected by the end of 2011, and the company is confident it will bring innovation to the generic test bench concept. ▮

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