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Open-People: Open Power and Energy Optimization PLatform and Estimator

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***Abstract*—Designing low power complex embedded systems is now a critical challenge for a large number of electronic corporations. Low power is generally critical due to its impact on lifetime, battery longevity, battery capacity, temperature constraints, etc. Unfortunately, when a designer needs some power estimations about its design, the methods and tools which can help him are not sufficient. Indeed, there is a lack of efficient methodology and accurate tool to obtain power/energy estimation of a complete system at different abstraction levels. This paper addresses this problem and proposes a global framework for power/energy estimation and optimization of heterogeneous MultiProcessor System on Chip (MPSoC). This framework supports both a power modeling methodology and a power platform estimations which can help the designer to choose the best solution for his design. The methodology supported takes into account all the embedded system's relevant aspects; the software, the hardware, and the operating system. It includes several estimation tools with respect to their abstraction levels in order to cover the overall design flow. Starting from functional estimation and down to real boards measurements, our platform helps designers to develop new power models, to explore new architectures, and to apply optimization techniques in order to reduce energy and power consumption of the system. The usefulness and the effectiveness of the proposed power estimation framework are demonstrated through a typical embedded system conceived around the Xilinx Virtex II Pro FPGA platform.**

***Keywords*-**

I. INTRODUCTION

The increasing complexity of applications and System-on-Chip (SoC) architectures places embedded system designers in front of a very large design space. In this context, exploring the design space to reach an efficient solution becomes very difficult, and this is particularly difficult when the design must satisfy a large number of constraints, such as power and energy consumption. These constraints have led to introduce the usage of Multi-Processor System-on-Chip (MPSoC) which allow to integrate very complex systems, including reconfigurable execution resources. These MPSoCs are generally heterogeneous and can contain memories (Cache, SRAM, FIFO, etc.), processors (GPP, DSP, etc.), interconnecting elements (Bus, Crossbar, NoC, etc.), I/O peripherals, and reconfigurable logic. To use the tremendous hardware resources available in next generation MPSoCs efficiently, rapid and accurate design space exploration (DSE) methods are needed to evaluate the different design alternatives and to help the designer during the design steps. MPSoCs must be designed with custom architectures to balance the implementation constraints between the application needs (i.e. high computation rates and low power consumption) and the production cost. Nevertheless, the significant increase of complexity in such systems prevents designers from controlling the complete design flow, and design abstraction is very critical to guide the designer during the different design choices. To be acceptable, the abstraction must include all the system-on-chip aspects, i.e. architecture/hardware, application/software, and management/operating system. Furthermore, the associated tools must be able to provide results from several description levels of the in-development system. Indeed, during the first design steps, designers have a very high description granularity of each part of the corresponding system. Nevertheless, first evaluations of power consumption can be necessary to make rapid and reliable design choices. This permits a rapid exploration of a large solution space by eliminating non-interesting regions from the DSE process. Gradually, the possible alternatives will be reduced by refinement of each part of the system. At a lower design step, the designer needs more accurate tools to explore the selected solutions in order to locate the most power-efficient configurations. At each step, different power evaluations can be extracted from a software or a hardware component relying on parametric power consumption models.

This paper addresses this problem and proposes an efficient methodology and associated tools for power estimation and optimization. The methodology proposed is embedded

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in a open platform [1] which support a complete framework to ease the design of complex systems. It aims at providing a complete framework i) to allow rapid power/energy estimation for complex heterogeneous systems, ii) to test different optimizations in order to significantly reduce the power consumption of the system.

The goal of the Open-People platform is to provide an access to hardware execution boards (processor, dsp, fpga, logic analyzers, etc.) and the control of power estimations and optimizations.

Through a secured web portal, the platform provides an access to the power measurements and helps the designer to define models of energy consumption for hardware and software components of a complete system. These models can be included in the component library in order to be used for estimation and optimization design steps. At the end of Open-People project, the platform will propose a set of optimization tools at different levels of description and/or for the different target boards (architectural optimizations, operating system optimizations, etc).

Addressing high levels of abstraction helps solving this problem, but it must also permit the evaluation and estimation of performances for the system under design. Thus, the high level abstraction must also support model transformation and code generation to execute and/or synthesize different parts of the system.

In the context of embedded systems, one of the most important constraints is the power consumption. Some others constraints like memory size or processor performances also need to be addressed to ensure that the final product will satisfy the requirements. To help the designer in exploring the design space, it becomes more and more important to provide methods and tools for early estimations of the system's characteristics (performance, power). Several methods and tools have been developed for that, but none of them proposes to model the reconfiguration aspects of System-on-Chips.

This paper is organized as follows. Section II presents the state of the art of methods and tools for modeling embedded systems. Section III presents the platform OPEN-PEOPLE and explains how this platform can be used to explore different implementations of software and hardware solutions. Finally, Section IV concludes this paper.

II. STATE OF THE ART

Significant research efforts have been devoted to develop tools for power consumption at the different abstraction levels in embedded system design. Among the existing tools for low abstraction levels, we can mention SPICE [1], Diesel [2], and PETROL [2] which operate at the RTL level. These tools are fairly accurate, but require significant amount of simulation time. At such low level, tools are used to optimize power consumption of hardware blocks but not to evaluate entirely complex SoC architectures.

To cope with the evaluation time, several tools have been developed for power consumption estimation at the system level. Among the wide-used approaches, we quote tools based on micro-architectural cycle-level simulation such as Wattch [3] and Simplepower [4]. They define fine-grain power models by characterizing component features such as a set of instructions or functional blocks using analytic power laws. The contributions of the internal unit activities are calculated and added together during the execution of the program on the micro-architectural simulator. This approach needs low-level description of the architecture which is often difficult to obtain for off-the-shelf processors. Though using cycle-level simulators allows accurate power estimation, the simulation time of complex MPSoC needed to achieve the results is still long.

In an attempt to reduce simulation time, recent efforts have been done to build up fast simulators using *Transaction Level Modeling* (TLM) [5] [6]. SystemC [7] and its TLM 2.0 kit have become a de facto standard for the system-level description of SoCs. The TLM kit proposes different coding styles to offer concepts for loosely and approximately timed models. However, there is not a standard definition for concepts or methodologies that involves power estimation at the TLM level and this aspect is still under research and is not well established. In [8] and [9], a methodology is presented to generate consumption models for peripheral devices at the TLM level. Relevant activities are identified at different levels and granularities. The characterization phase is however done at the gate level from where the activity and power consumption for the higher level are deduced. Using this approach for recent processors and systems is not realistic.

For the functional level, Tiwari et al. [10] have introduced the concept of Instruction Level Power Analysis (ILPA). They associate a power consumption model with instructions or instruction pairs, which are characterized using measurements on a real chip. This approach suffers from the high number of experiments required to obtain the model. In addition, it can be applicable only for processors. To overcome this drawback, Laurent [11] et al. proposed the *Functional Level Power Analysis* (FLPA) methodology that was successfully applied on building high-level power models for different hardware components (processor, memory, I/O peripherals, FPGA, etc.). FLPA relies on the identification of a set of functional blocks which influence the power consumption of the target component. The model is represented by a set of analytical functions or a table of consumption values which depend on functional and architectural parameters. Once the model is build, the estimation process consists of extracting the appropriate parameter values from the design, which will be injected into the model to compute the power consumption. Based on

[1] www.open-people.fr

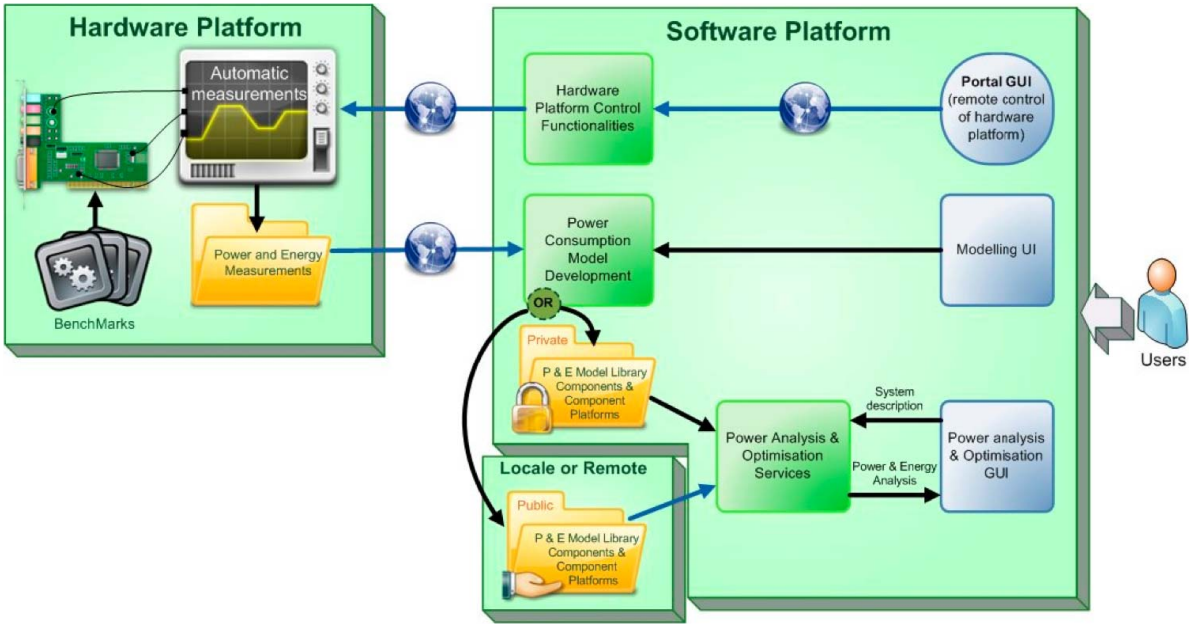

Figure 1. Global view of the OPEN-PEOPLE platform.

this methodology, the tool SoftExplorer [12] was developed. It includes a library of power models for simple to complex processors. Recently, SoftExplorer has been included as a part of Consumption Analysis Toolbox (CAT) [13].

For the reconfigurable circuits (FPGA), several studies have been done during last years. One of the first modeling proposal has been done in by Garcia et al. in [**?**], [**?**]. In these works, the power modeling is measured for the different elements of the circuit (LUT, register, I/O, clock tree, etc). The power consumption measured in this work concerns the active component, but the configurable memory is not considered, and the reconfiguration aspect is not evaluated. In [**?**], authors explain how the pipeline of some hardware functions can reduce the power consumption by the reduction of the clock frequency. High-level estimations have also been developed for this type of circuit. For example, the works presented in [**?**] and [**?**] propose to model the power by using high level characteristics of the system. In [**?**], the signal statistics are used to extract the activity and then compute the power consumption of each hardware block. A composition of these consumptions enables to evaluate the global consumption of the system. In [**?**], the high level characteristics of the functionality is used to model the power consumption. For example, the frequency of the hardware implementation of a functionality is used to estimate the power/energy consumption, and a sum of all the power consumed in the circuit enables to evaluate the power/energy of the system. When considering operating system level, the service which ensures the task scheduling and the task placement have an impact on the power consumption, and in particular on the static power consumption.

Several works have studied this impact without actually proposing consumption models. [14] and [15] have shown that the energy consumption can rise from 6% to 50% with an OS, depending on the application, and that it increases with the processor frequency and supply voltage. [16] has shown that the OS can consume from 1% to 99% of the processor energy depending on the services called. Actual consumption models are only proposed in a few works [17], [18], or [19]. They however only consider simple systems or only sub parts of the operating systems functionality or services, and furthermore may be again limited by the accuracy of the energy simulators used.

In the frame of the OPEN-PEOPLE project, the particularity of our approach is that it is based on actual measurements on the electronic boards, and that it aims at proposing consumption models for every component in the embedded systems considered. Following this direction, we propose models to take into account complete real-time embedded systems, including complex processors, reconfigurable components (FPGA), and dedicated OS services such as scheduling, context switching, or inter-process communications [13], [20].

III. OPEN-PEOPLE PLATFORM PRESENTATION

A. Hardware part of the platform

OPEN-PEOPLE stands for Open Power and Energy Optimization PLatform and Estimator. The platform is defined for estimation and optimization of the power and energy

consumption of complex electronic systems. The figure 1 presents a global view of the platform which is based on two main parts; the software part and the hardware part. The software user interface ensures the access to the power measurements and helps the designer to define energy models for the hardware and software system components. From the measurements, the designer can build models and compute an estimation of the energy and/or power consumption of its system. In addition, from this software user interface, the hardware platform can be controlled. The hardware part consists of the embedded system boards, the measurement equipments, and the computer that controls these different elements and schedules the list of measurements required by different users.

Among the target systems, we mention heterogeneous MPSoCs such as the TI OMAP 3530 [21] and reconfigurable circuits like the Xilinx Virtex5 FPGA [22]. Our platform allows power estimation using:

- direct access to the hardware execution boards and the measurement equipments. This first alternative enables the designer to measure the real power dissipation of the target system. To do so, the low level description of the system (C, VHDL, etc.) is carried out natively on the target board. Furthermore, this alternative is used to build new power models for hardware or software components. Several boards have been integrated in our automated bench and equipped with special gear to allow for power consumption measurement. Among those boards, one may find some processor based boards or some FPGA based boards. The figure 2 shows the global hardware structure of the complete platform. This platform is based on several electronics equipments for power supply, power analysis and interconnection between the different equipments. All these elements are connected to a workstation which is responsible of managing the different power consumption measurements.
  The complete list of the available boards is presented below:
  - OMAP3530 EVM (ARM Cortex A8 + DSP C64) ;
  - Xilinx SP605 (SPARTAN 6) ;
  - Xilinx ML550 (VIRTEX 5) ;
  - Xilinx XUPV2P ;
  - Altera Cyclone III LS.
- a set of Electronic System Level (ESL) tools coupled with accurate power models elaborated within the first alternative. Mainly, we offer tools at the functional and transactional levels in the context of multilevel exploration of new complex architectures.

The figure 3 presents an overview of the hardware platform located at Lorient, in France. On this figure, we can show one specific board under test in order to measure the power consumption. The top of the figure shows the Power Analyzer N6705A from Agilent and the bottom shows the XupV2Pro board from Xilinx.

Figure 3. Photo of a part of the hardware platform Open-People.

B. Software part of the platform

In the frame of the OPEN-PEOPLE project, new methods and tools to model the different components of an heterogeneous system architecture are proposed including processors, hardware accelerators, memories, reconfigurable circuits, operating system services, IP blocks, etc. For reconfigurable systems, the dynamic reconfiguration paradigm will be modeled to estimate how this feature can be used by the Operating System (OS) and to reduce the energy consumption. Furthermore, this project studies how the complete estimation and validation can be performed for very complex systems with a small simulation time.

In order to fill the AADL model with power consumption information, the platform offers some specific interfaces to specify both mathematical equations or list of points (LUT). The figures 4 and 5 show two examples of these interfaces. The designer can use one of these interfaces, depending on the power consumption model of each block. The definition of equations is based on several other specifications like unit specification, or more generally from any quantity specifications.

C. Methodology

The global methodology of this platform is based on the AADL language, and enables to decompose the design in several parts, which are the software part, the hardware part and the deployment of the application on the hardware. This global flow is illustrated on the figure 6. This flow includes

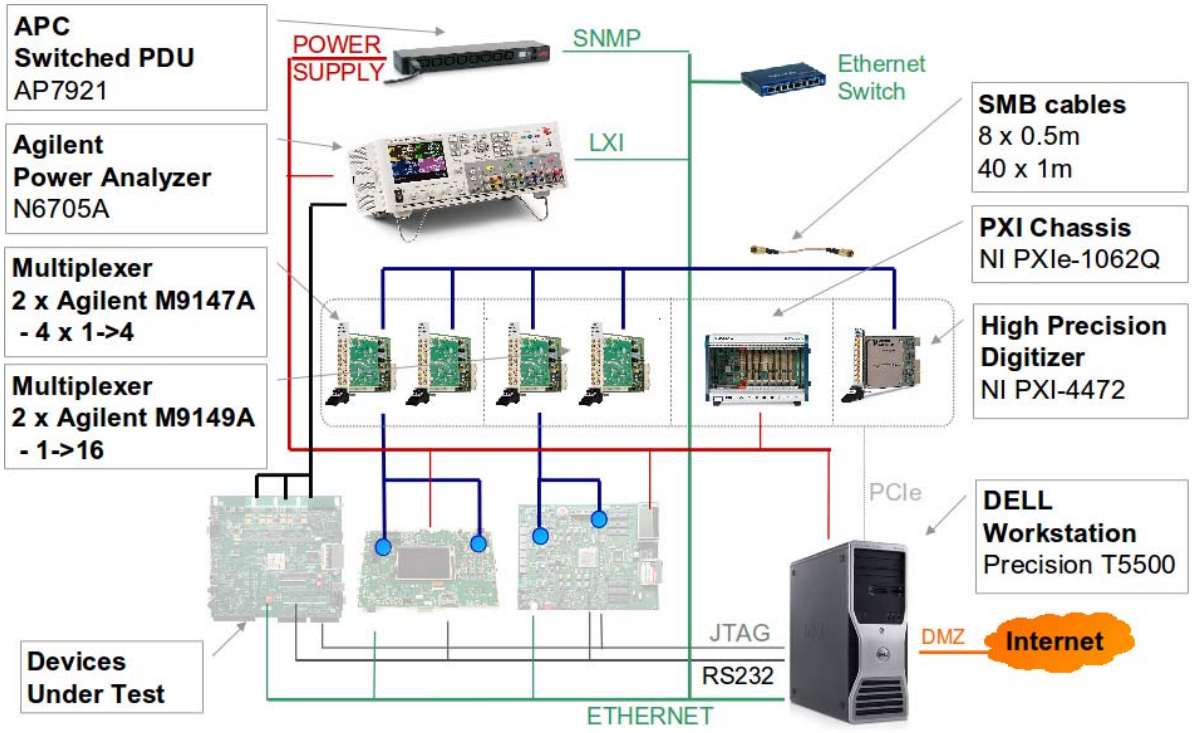

Figure 2. Global organization of the hardware resources available in the Open-PEOPLE platform.

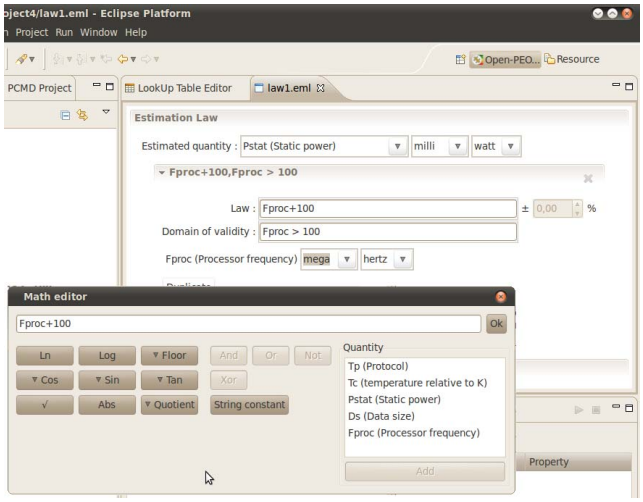

Figure 4. Interface to specify power consumption as equation for a specific block.

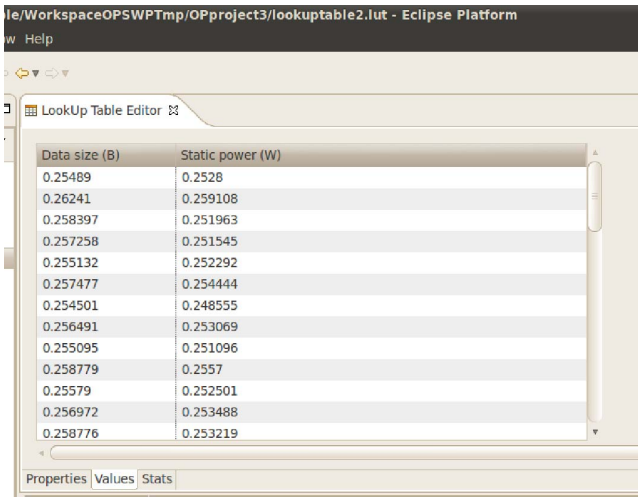

Figure 5. Interface to specify power consumption as look up table for a specific block.

the model of the application, as a set of tasks. These tasks must be defined by a set of parameters, including real time constraints. The flow also includes a power model of each hardware element of the platform. Finally, to offer execution flexibility, the tasks can be described by several different implementations, defined by different characteristics.

From the definition of i) all the hardware blocks available in the architecture, ii) all the tasks if the application, iii) different implementations of some tasks (or all tasks) to offer flexibility, the methodology consists on evaluating the power consumption impact of a designer's choices. From one specific task graph, it is then possible to explore the

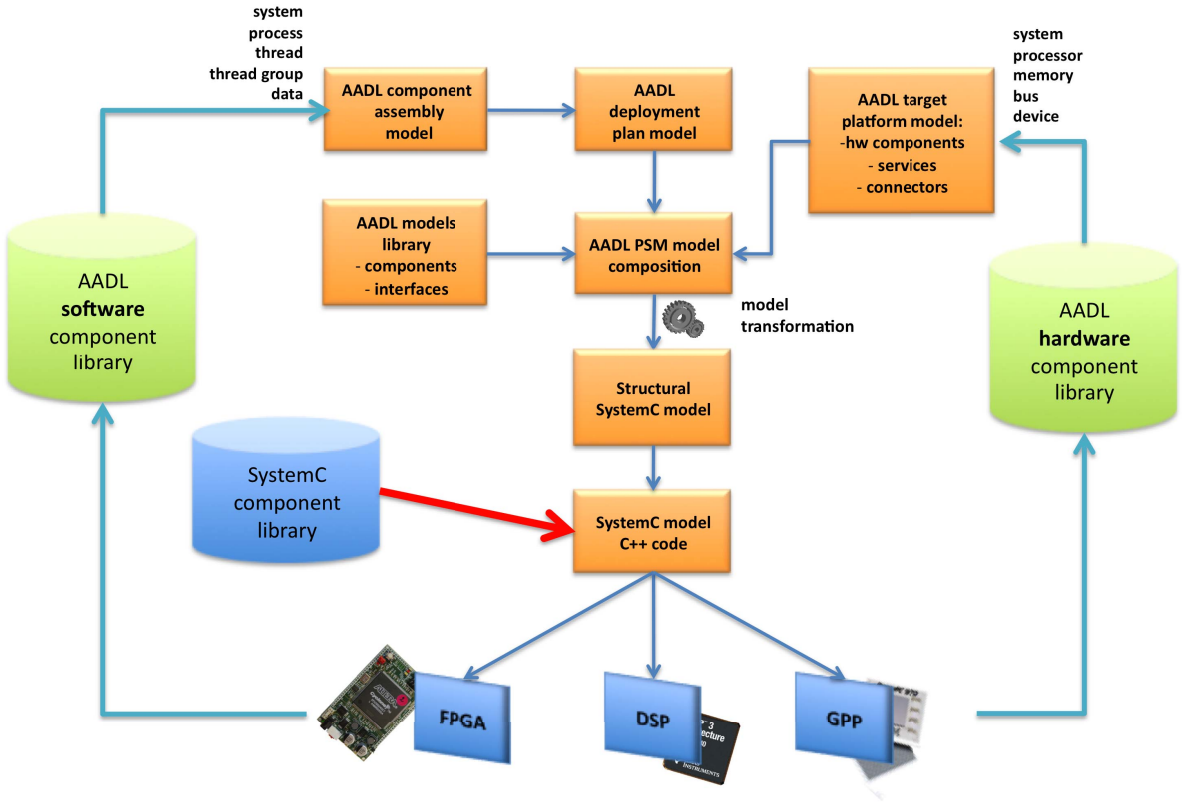

Figure 6. Design flow based on AADL language.

cost of a solution where all the tasks are implemented as software tasks running on processor, or as hardware tasks running as specific accelerators. Between these two extreme solutions, the designer can evaluate all the other solutions, and choose the one which is the best due the constraints of the design that best suits to the constraints of the design.

As an example of output results which can be provided by the platform, we briefly present two solutions for the implementation of the application H264 decoder. This application is composed of several tasks, which can be represented as shown in figure 7

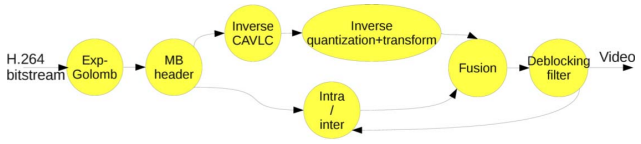

Figure 7. Design flow based on AADL language.

For this task graph, all the tasks are described as software and for tasks that can be executed on a processor, and some of these tasks can be executed as hardware accelerators on reconfigurable resources. These different implementations are described in the tables I and II.

Task	Time (ms)	Energy (mJ)
ExGolomb	45	180
MBHeader	60	240
Cavlc	110	440
QtTr	50	200
Intra	55	220
Deblock	175	700

Table I
EXECUTION TIMES AND POWER CONSUMPTIONS OF SOFTWARE VERSIONS OF THE TASKS FOR H264 DECODER APPLICATION.

Task	Impl	A (slice)	Time (ms)	Energy (mJ)	Idle (mW)
Cavlc	1	3700	74.8	15.2	20
	2	3800	71	14.6	21
QtTr	1	1000	30.5	2.9	9
	2	1200	24.1	2.5	10
Deblock	1	2849	21	1.5	51.2
	2	2880	16.6	1.2	53

Table II
EXECUTION TIMES AND POWER CONSUMPTIONS OF HARDWARE VERSIONS OF THE TASKS FOR H264 DECODER APPLICATION.

From the power consumption parameters that are also present in this characterisation, the goal is to decide which tasks will be executed on processors and which tasks will be executed on reconfigurable resources. The methodology developed in the project OPEN-PEOPLE enables to extract the results as shown in figure 8.

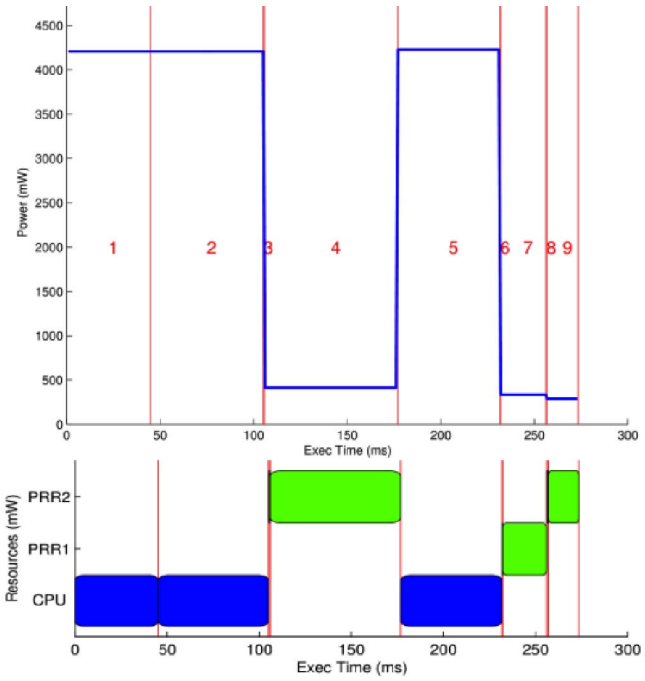

Figure 8. Task scheduling of the H264 decoder application for the fastest solution.

This figure presents an example of task instantiation on a system composed of a processor and reconfigurable logic. The top of this figure shows the power consumption while the bottom shows the tasks scheduling. From this type of graphics, the designer can evaluate several points which are the execution time, the maximum power consumption of his design, and the total energy consumption of the execution of the application.

Other combinations of task instantiations can be explored if necessary and when one specific combination is chosen the designer can refine his design in order to obtain more accurate performance estimations.

IV. CONCLUSION

This paper has presented a platform defined to help the electronics designers during the design steps. The platform mainly addresses the low power constraint of large number of embedded systems developed today. It is composed of an hardware part which enables real low power measurements on real electronics boards. These measurements are available through an open software platform which proposes the management of the measurement campaigns and the access to power estimator and optimization tools.

From these real measurements, the platform enables to derive relevant AADL models of all the components (software and/or hardware), and these power properties are then used to explore different solutions for tasks implementations.

To ensure secure access to the platform, the platform provides authentication mechanisms, and the platform can be used as a standalone tool on a personnel computer if high security is needed for the application and/or architecture confidentiality reasons.

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