Massively Parallel Dynamically Reconfigurable Multi-FPGA Computing System

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***Abstract*—High Performance Embedded Computing (HPEC) applications are becoming highly sophisticated as they capture and process real-time data from several sources. In addition, they should adapt their functionalities according to the operational environments. The inherent hardware parallelism that allows Single Program Multiple Data (SPMD) execution model, high-speed serial I/O and Dynamic Partial Reconfiguration (DPR) features make FPGAs a highly attractive solution. The problem with current generation reconfigurable HPEC systems is that, they are usually built to meet the needs of a specific application i.e., lacks flexibility to upgrade hardware resources or adaptability to different applications. In order to address these challenges, we propose a scalable and modular multi-FPGA computing platform, with a parallel full-duplex customizable communication network, that redefines the computation, communication and reconfiguration paradigms in such applications. Furthermore, in order to adapt to real-time application constraints, we propose a parallel DPR model. It is well-traced on the execution model (SPMD), to reconfigure all or a subset of the computing nodes in parallel during runtime.**

***Keywords*-Parallel and dynamic computing; Multi-FPGA; scalable architecture; parallel reconfiguration;**

I. Parallel and Scalable Reconfigurable Architecture

In order to provide modular and customizable computing power, we have decoupled the FPGAs from the rest of the Printed Circuit Board (PCB), using a high-density array connector. Our parallel reconfigurable architecture consists of 4 detachable FPGA modules, along with DDR3 memory and a FPGA Mezzanine Card(FMC) [1] interface per module. Any I/O interface required for an application can be provided via an FMC module [1]. High-bandwidth low-latency communication is provided using a PCIe Gen3 switch. This allows seamless data and I/O sharing among computing peers. Finally, there is also a detachable processor / host module that will be the root complex for all the FPGA nodes in the PCIe tree.

The host to FPGA PCIe communication and parallel execution support is provided using an open-source XillyBus PCIe [2] and POSIX Libraries and drivers from PicoComputing [3]. Thus the host and the FPGAs can communicate with more than 1 FPGA at the same time, via the PCIe switch and the PThread library. Using these features, we have implemented a parallel, scalable and distributed H.264 encoding and encryption application as shown in Fig. 1. Based on the SPMD execution model, the number of nodes can be customized depending on the number of video channels. The encryption and encoding algorithms on all the nodes can be swapped for another in parallel, during runtime if required.

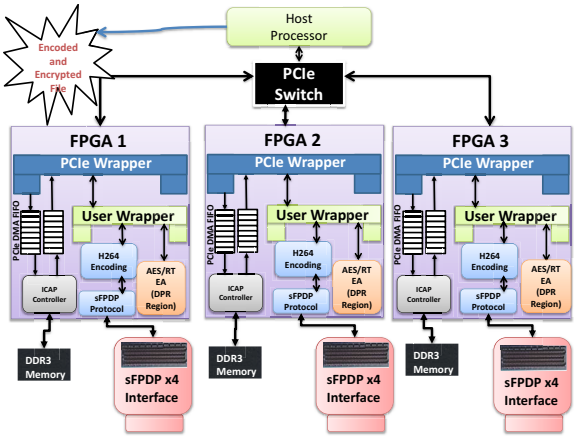

Fig. 1: Scalable distributed secure H.264 encoding on a multi-FPGA system

It has been demonstrated that DPR can provide modular I/O interfaces using FMC [2]. The performance metrics of the proposed architecture demonstrates hardware virtualization [3] using DPR on commercial HPEC applications. These results represent a conceptual proof for a massively parallel dynamically reconfigurable next generation HPEC system.

[1] http://www.vita.com/FMC
[2] http://xillybus.com/
[3] http://picocomputing.com/

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